REMARKS/ARGUMENTS

Claims 1 and 3-24 are pending in this application. By this Amendment, Applicants amend claims 1, 6, 8, 9, 13, 15 and 24 and cancel claims 2 and 25-30.

Applicants affirm the election of claims 1-24 directed to a method of making a semiconductor device without traverse. Accordingly, Applicants have canceled non-elected claims 25-30. Applicants reserve the right to file a Divisional Application to pursue prosecution of non-elected claims 25-30.

The Examiner indicated that the IDS filed on January 26, 2004 (certificate of mailing dated January 22, 2004) has not been considered because it allegedly contained an incorrect serial number (10/643,961). Applicants submit herewith a copy of the IDS filed on January 22, 2004, including a copy of the postcard stamped by the USPTO, which indicates that the USPTO received the IDS, including the correct serial number 10/647,696, on January 26, 2004. Applicants respectfully submit that the incorrect serial number was a result of an error on the part of the USPTO. Accordingly, Applicants respectfully request that the enclosed IDS be considered, and that the Examiner include an initialed and signed copy of the PTO-1449 with the next Office Action.

Claim 6 was objected to for containing a minor informality. Applicants have amended claim 6 to correct the informality noted by the Examiner. Accordingly, Applicants respectfully request reconsideration and withdrawal of this objection.

Claims 13 and 24 were rejected under 35 U.S.C. § 112, second paragraph, for allegedly being indefinite. Applicants have amended claims 13 and 24 to correct the informalities noted by the Examiner. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 1, 4-7 and 10-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Atwood et al. (U.S. 6,656,770) in view of Tonti et al. (U.S. 5,773,362). Claims 2, 8, 9 and 13-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Atwood et al. in view of Tonti et al., and further in view of Sono et al. (U.S.

5,444,025). Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Atwood et al. in view of Tonti et al., and further in view of Huang et al. (U.S. 2002/0180035). Claim 2 has been canceled. Applicants respectfully traverse the rejections of claims 1 and 3-24.

Claim 1 has been amended to recite:

"A process for manufacturing an integrated circuit package comprising:

mounting a semiconductor die, to a first surface of a substrate such that bumps on said semiconductor die are electrically connected to conductive traces of said substrate;

mounting at least one collapsible spacer to at least one of a heat spreader, said semiconductor die and said substrate;

fixing said heat spreader to at least one of said first surface of said substrate and said semiconductor die such that said at least one collapsible spacer is disposed therebetween;

forming a ball grid array on a second surface of said substrate, bumps of said ball grid array being electrically connected to said conductive traces; and

singulating said integrated circuit package,

wherein fixing said heat spreader comprises:

placing one of said heat spreader and said substrate in a mold cavity of a mold;

releasably clamping the other of said heat spreader and said substrate to a die of said mold cavity, such that said at least one collapsible spacer is disposed between said heat spreader and said substrate; and

molding a molding compound in the mold cavity, thereby molding the semiconductor die, the substrate, said at least one collapsible spacer and said heat spreader into the molding compound to provide a molded package." (emphasis added)

Claim 15 recites features and method steps that are similar to the features and method steps recited in claim 1, including the above-emphasized features.

With the improved features and method steps of claim 1, including the steps of "mounting a semiconductor die, to a first surface of a substrate such that bumps on said semiconductor die are electrically connected to conductive traces of said substrate,"

"placing one of said heat spreader and said substrate in a mold cavity of a mold," "releasably clamping the other of said heat spreader and said substrate to a die of said mold cavity, such that said at least one collapsible spacer is disposed between said heat spreader and said substrate," and "molding a molding compound in the mold cavity, thereby molding the semiconductor die, the substrate, said at least one collapsible spacer and said heat spreader into the molding compound to provide a molded package," Applicants have been able to provide a method for manufacturing an integrated circuit package in which a semiconductor die mounted on a substrate and a heat spreader are incorporated into a package during manufacture, which produces an integrated circuit package having enhanced thermal characteristics (see, for example, paragraph [0002] on page 1 and paragraph [0012] on page 3 of the originally filed specification).

Claim 1 has been amended to recite the features and method steps recited in originally filed claim 2.

The Examiner acknowledged that "Atwood [et al.] in view of Tonti [et al.] do not disclose molding said die, said substrate, said collapsible spacer, and said heat spreader in a molding compound." The Examiner alleged that "Atwood [et al.] and Tonti [et al.] would look to one such as Sono [et al.] for device protection because Sono discloses wherein fixing said heat spreader comprises: placing one of said heat spreader and said substrate in a mold cavity (Fig. 3B); releasably clamping the other of said heat spreader and said substrate to a die of said mold cavity, such that collapsible spacer is disposed between said heat spreader and said substrate (col. 4 lines 16-20); and molding a molding compound in the mold, thereby molding the semiconductor die, the substrate, said at least one collapsible spacer, and said heat spreader into the molding compound to provide a molded package (Fig. 6 el. 7)." Thus, the Examiner concluded that it would have been obvious to "use the molding of Sono [et al.] with the process of Atwood [et al.] in view of Tonti [et al.] in order to protect the device from moisture, and chemical and mechanical stress; and to provide highly accurate

placement of the heatsink." Applicants respectfully disagree.

Atwood et al. teaches the use of a solder 18 that is in a semi-molten state to fix a heat exchanger unit 14 to an integrated circuit chip 12 and substrate 10. The semi-molten solder 18 is used to reduce stresses induced by the differences in the coefficients of thermal expansion between the heat exchanger unit 14 and the integrated circuit chip 12 and between the heat exchanger unit 14 and the substrate 10.

Atwood et al. clearly fails to teach or suggest **any** of the steps of "placing one of said heat spreader and said substrate in a mold cavity of a mold," "releasably clamping the other of said heat spreader and said substrate to a die of said mold cavity, such that said at least one collapsible spacer is disposed between said heat spreader and said substrate," and "molding a molding compound in the mold cavity thereby molding the semiconductor die, the substrate, said at least one collapsible spacer and said heat spreader into the molding compound to provide a molded package" as recited in claim 1, and similarly as recited in claim 15.

Tonti et al. merely teaches a heat sink 61 that is attached to a traditional integrated circuit package 12 using a thermal adhesive 13.

Thus, Tonti et al. also completely fails to teach or suggest **any** of the steps of "placing one of said heat spreader and said substrate in a mold cavity of a mold," "releasably clamping the other of said heat spreader and said substrate to a die of said mold cavity, such that said collapsible spacer is disposed between said heat spreader and said substrate," and "molding a molding compound in the mold cavity thereby molding the semiconductor die, the substrate, said at least one collapsible spacer and said heat spreader into the molding compound to provide a molded package" as recited in Applicants' claim 1, and similarly as recited in Applicants' claim 15.

Sono et al. teaches a method of producing a semiconductor device in which a semiconductor chip 5 is mounted on a top surface of a "radiator block 3" and electrically connected to the leads 2. The radiator block 3 is located on a lower die 24b and an

upper die 24a is disposed on top of the lower die such that the leads 2 extend from an interior cavity of the lower and upper dies 24b, 24a to an exterior thereof.

In contrast to Applicants' claimed invention, Sono et al. completely fails to teach the steps of "placing one of said heat spreader and said substrate in a mold cavity of a mold," "releasably clamping the other of said heat spreader and said substrate to a die of said mold cavity, such that said at least one collapsible spacer is disposed between said heat spreader and said substrate," and "molding a molding compound in the mold cavity thereby molding the semiconductor die, the substrate, said at least one collapsible spacer and said heat spreader into the molding compound to provide a molded package" as recited in Applicants' claim 1, and similarly as recited in Applicants' claim 15.

Furthermore, Sono et al. fails to teach or suggest any step of "mounting a semiconductor die, to a first surface of a substrate such that bumps on said semiconductor die are electrically connected to conductive traces of said substrate" as recited in Applicants' claim 1, and similarly as recited in Applicants' claim 15. In fact, Sono et al. completely fails to teach or suggest the use of **any** substrate. Instead, Sono et al. teaches that the semiconductor die 5 is **directly** mounted to the radiator block 3. Thus, there is absolutely **no** substrate to which the semiconductor die is mounted, as recited in Applicants' claims 1 and 15.

The fact that Sono et al. fails to teach or suggest any substrate appears to be one of the keys to the Sono et al. package since the heat from the semiconductor die 5 is radiated through the "radiator block" which acts as a heat spreader. Thus, Sono et al. clearly teaches that the semiconductor die 5 **must** be mounted on the heat spreader, and thus, the semiconductor die 5 of Sono et al. **cannot** be mounted on a substrate.

Since there is no substrate taught or suggested in the molded package of Sono et al., Sono et al. cannot possibly teach the steps of "placing one of said heat spreader and **said substrate** in a mold cavity of a mold," "releasably clamping the other of said heat spreader and **said substrate** to a die of said mold cavity, such that said at least

one collapsible spacer is disposed between said heat spreader and **said substrate**," and "molding a molding compound in the mold cavity thereby molding the semiconductor die, **the substrate**, said at least one collapsible spacer and said heat spreader into the molding compound to provide a molded package" as recited in Applicants' claim 1, and similarly as recited in Applicants' claim 15.

Sono et al. teaches the use of a semiconductor die 5, a radiator block 3, and leads including inner lead portions 2A and outer lead portions 2B, which are molded in a molding compound. However, Sono et al. clearly fails to provide any teaching or suggestion of a substrate that is molded in the package shown in Figures 1-5. In fact, a circuit substrate 100 is shown in Fig. 6 of Sono et al. As shown and described in Sono et al., the circuit substrate 100 is entirely external to the molding compound and does not form any part of the package. Thus, not only does Sono et al. fail to teach or suggest the step of "molding a molding compound in the mold cavity, thereby molding the semiconductor dies, the substrate, said at least one collapsible spacer and said heat spreader into the molding compound to provide a molded package" as recited in Applicants' claim 1, and similarly as recited in Applicants' claim 15, but Sono et al. also clearly teaches away from the molding step recited in Applicants' claim 1, and similarly as recited in Applicants' claim 15, because in the structure of Sono et al., the substrate 100 is clearly entirely external to the molding compound, does not form any part of the package, and **cannot** be included in the package. The Examiner is reminded that it is error to find obviousness where references diverge and teach away from the invention at hand. W.L. Gore & Assoc. v. Garlock Inc., 220 USPQ 303, 311 (Fed. Cir. 1983).

Thus, Applicants respectfully submit that none of Atwood et al., Tonti et al. and Sono et al. teaches or suggests the steps of "placing one of said heat spreader and said substrate in a mold cavity of a mold," "releasably clamping the other of said heat spreader and said substrate to a die of said mold cavity, such that said collapsible spacer is disposed between said heat spreader and said substrate," and "molding a molding compound in the mold cavity thereby molding the semiconductor die, the

substrate, said at least one collapsible spacer and said heat spreader into the molding compound to provide a molded package" as recited in Applicants' claim 1, and similarly as recited in Applicants' claim 15.

Accordingly, Applicants respectfully submit that Atwood et al., Tonti et al. and Sono et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of method steps and features recited in Applicants' claims 1 and 15.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Atwood et al., Tonti et al. and Sono et al.

In view of the foregoing amendments and remarks, Applicants respectfully submit that Claims 1 and 15 are allowable. Claims 3-14 and 16-24 depend upon claims 1 and 15, and are therefore allowable for at least the reasons that claims 1 and 15 are allowable.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Date: September 20, 2004

Attorneys for Applicant

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

KEATING & BENNETT LLP
10400 Eaton Place, Suite 312
Fairfax, VA 22030
Telephone: (703) 385-5200
Facsimile: (703) 385-5080